IN THE CLAIMS

Please amend the claims as follows:

Claim 1-2 (Canceled)

Claim 3 (Previously Presented): A signal processing circuit of an image input apparatus, comprising:

first and second register groups provided with a plurality of storage regions of the same number of bits as a unit image signal in predetermined units that is obtained by an image pickup device in said image input apparatus and arranged in two dimensions, said first and second register groups having first to fourth registers, respectively, said first to fourth registers having zero-th to third storage regions, respectively,

wherein said zero-th storage regions of said first to fourth registers of said first register group are connected directly, by a predetermined connecting line, to said zero-th to third storage regions of said fourth register of said second register group,

said first storage regions of said first to fourth registers of said first register group are connected directly, by a predetermined connecting line, to said zero-th to third storage regions of said third register of said second register group,

said second storage regions of said first to fourth registers of said first register group are connected directly, by a predetermined connecting line, to said zero-th to third storage regions of said second register of said second register group, and

said third storage regions of said first to fourth registers of said first register group are connected directly, by a predetermined connecting line, to said zero-th to third storage regions of said first register of said second register group.

Claim 4 (Previously Presented): A signal processing circuit of an image input apparatus, comprising:

first and second register groups provided with a plurality of storage regions of the same number of bits as a unit image signal in predetermined units that is obtained by an image pickup device in said image input apparatus and arranged in two dimensions, said first and second register groups having first to fourth registers, respectively, said first to fourth registers having zero-th to third storage regions, respectively,

wherein said zero-th storage regions of said first to fourth registers of said first register group are connected directly, by a predetermined connecting line, to said zero-th to third storage regions of said fourth register of said second register group,

said first storage regions of said first to fourth registers of said first register group are connected directly, by a predetermined connecting line, to said zero-th to third storage regions of said third register of said second register group,

said second storage regions of said first to fourth registers of said first register group are connected directly, by a predetermined connecting line, to said zero-th to third storage regions of said second register of said second register group, and

said third storage regions of said first to fourth registers of said first register group are connected directly, by a predetermined connecting line, to said zero-th to third storage regions of said first register of said second register group; and

a third register group having first to fourth registers which are respectively provided with zero-th to third storage regions of the same number of bits as a unit image signal in predetermined units arranged in two dimensions,

wherein said zero-th to third storage regions of said first register of said second register group are connected directly, by a predetermined connecting line, to said third to zero-th storage regions of said first register of said third register group, respectively,

said zero-th to third storage regions of said second register of said second register group are connected directly, by a predetermined connecting line, to said third to zero-th storage regions of said second register of said third register group, respectively,

said zero-th to third storage regions of said third register of said second register group are connected directly, by a predetermined connecting line, to said third to zero-th storage regions of said third register of said third register group, respectively, and

said zero-th to third storage regions of said fourth register of said second register group are connected directly, by a predetermined connecting line, to said third to zero-th storage regions of said fourth register of said third register group, respectively.

Claim 5 (Original): A signal processing circuit of an image input apparatus, comprising:

second and third register groups provided with a plurality of storage regions of the same number of bits as a unit image signal in predetermined units that is obtained by an image pickup device in said image input apparatus and arranged in two dimensions, said second and third register groups having first to fourth registers, said first to fourth registers having zero-th to third storage regions,

wherein said zero-th to third storage regions of said first register of said second register group are connected directly, by a predetermined connecting line, to said third to zero-th storage regions of said first register of said third register group, respectively;

said zero-th to third storage regions of said second register of said second register group are connected directly, by a predetermined connecting line, to said third to zero-th storage regions of said second register of said third register group, respectively;

said zero-th to third storage regions of said third register of said second register group are connected directly, by a predetermined connecting line, to said third to zero-th

storage regions of said third register of said third register group, respectively; and

said zero-th to third storage regions of said fourth register of said second register group are connected directly, by a predetermined connecting line, to said third to zero-th storage regions of said fourth register of said third register group, respectively.

Claims 6-15 (Canceled)